WHAT IS CLAIMED IS:

1. In a multi-level memory array comprising a plurality of conductors on each level of the memory array, forming a memory cell at each intersection between conductors of adjacent levels, each cell having a respective directionality in common with cells of at least one adjacent level, a method of writing a selected memory cell comprising the steps of:

biasing a first conductor coupled to an anode terminal of the selected memory cell to a first voltage;

biasing a second conductor coupled to a cathode terminal of the selected memory cell to a second voltage lower than the first voltage;

biasing at least one of a group of unselected conductors on the same level as the first conductor to a third voltage between the first and second voltages and at an offset from the second voltage; and

biasing at least one of a group of unselected conductors on the same level as the second conductor to a fourth voltage between the first and second voltages and at an offset from the first voltage.

2. The method as defined in claim 1 further comprising allowing conductors on all other levels to float.

3. The method as defined in claim 1 wherein:

unselected conductors on all other levels beyond the cathode terminal of the selected memory cell are either biased or float to a voltage higher than a mid-point between the first and second voltages; and

unselected conductors on all other levels beyond the anode terminal of the selected memory cell are either biased or float to a voltage lower than the mid-point between the first and second voltages.

4. The method as recited in claim 1 further comprising biasing all unselected conductors on the same level as the first conductor to the third voltage.

5. The method as recited in claim 1 further comprising biasing all unselected conductors on the same level as the second conductor to the fourth voltage.

6. The method as recited in claim 5 further comprising biasing all unselected conductors on the same level as the first conductor to the third voltage.

7. The method as recited in claim 1 further comprising biasing unselected conductors on at least one other level beyond the level of the second conductor, relative to the selected cell, to a voltage higher than a mid-point between the first and second voltages.

8. The method as recited in claim 7 further comprising biasing unselected conductors on at least one other level beyond the level of the second conductor, relative to the selected cell, to the fourth voltage.

9. The method as recited in claim 1 further comprising biasing unselected conductors on at least one other level beyond the level of the first conductor, relative to the selected cell, to a voltage lower than the mid-point between the first and second voltages.

10. The method as recited in claim 9 further comprising biasing unselected conductors on at least one other level beyond the level of the first conductor, relative to the selected cell, to the third voltage.

11. The method as recited in claim 1 wherein a difference between the first voltage and the second voltage comprises a programming voltage having a magnitude of approximately 9 volts.

12. The method as recited in claim 1 wherein the offset of the third voltage from the second voltage has a magnitude of approximately 0.8 volts.

13. The method as recited in claim 1 wherein the offset of the fourth voltage from the first voltage has a magnitude in the range of 0.5-0.8 volts.

14. The method as recited in claim 1 wherein each memory cell includes an antifuse structure.